Study of different 3T-APS Pixel Configurations Using the Open Sky130 Process Design Kit

Luís Karlos Oliveira
Faculdade de Engenharia
Universidade Federal de Juiz de Fora
Juiz de Fora – MG, Brazil
luis.karlos@engenharia.ufjf.br

Estêvão Coelho Teixeira
Faculdade de Engenharia
Universidade Federal de Juiz de Fora
Juiz de Fora – MG, Brazil
estevao.teixeira@ufjf.br

Filipe Santos
Vinci Consulting
F-91192 Gif-sur-Yvette, France
filipe@laposte.net

***Abstract*—The Active Pixel Sensor (APS) is the core of modern CMOS imagers, which are currently present in almost all image acquisition applications. The key structure of an APS pixel is constructed using a photosensitive block and three readout transistors, known as the 3T pixel. In this work, we carry out a comparative study of different alternatives for implementing the 3T pixel using open source tools with the Sky130 technology. The readout circuit variants are composed by using several different MOSFET devices available from the open Sky130 Process Design Kit (PDK) and applying different supply, reset and row selection voltages, with the aim of obtaining the maximum possible linear voltage swing at the output. NGSPICE simulation results regarding linearity and output voltage swing are shown and discussed.**

***Index Terms*—CMOS image sensor, Active Pixel Sensor, Open PDKs, Sky130, Open Source Tools.**

I. Introduction

Active pixel sensors (APS) are the fundamental elements of modern CMOS imagers, today present in all advanced imaging systems (e.g. cell phone cameras, security, medical and scientific applications), among others [1]. The great advantage of APS CMOS technology is the integration into a chip containing sensors and all the readout electronics (all the analog, digital control, digitization and processing).

Since their invention in the 1990s, numerous publications have been produced, reporting improvements in several APS limitations, such as noise reduction [2], increased dynamic range [3] and use of In-pixel processing [4].

The fundamental APS pixel has, in addition to a photosensitive element, three MOSFETs working as an analog readout circuit (3T pixel). Better performance can be obtained by adding a transmission gate transistor, leading to the 4T pixel [5]. However, 4T pixels share the same inherent limitations of 3T pixels. There are pixels in which a higher number of transistors per pixel are used, in order to improve the sensor performance or even implement a in-pixel digitizing, reaching as many as 20 transistors per pixel [6]. The drawback of these complex pixels is the reduction on the fill factor, equivalent to the shrinking of the photosensitive area with respect to the overall pixel size, which is detrimental to imaging resolution.

This work is an investigation of different readout circuit configurations for the 3T-APS, using MOS devices available in the Sky130 CMOS fabrication technology [7], from SkyWater, using open source tools. The Sky130 is a mature, 180nm-130nm hybrid technology, which garnered interest in recent years due to the launching of the Sky130 Process Design Kit (PDK) with open access. This PDK was developed for use with open source design tools [8]. The Sky130 node offers several different MOS devices, intended for different levels of voltage supplies. This allows various APS readout combinations, which are evaluated in this paper w.r.t. the achievable linearity and output voltage swing. The simulation results were obtained by NGSPICE, using the transistor models contained in the open source PDK.

The rest of this paper contains four sections. In Section II, the 3T structure is described, and the different configurations are presented. In Section III, simulation results are detailed. A discussion about the results is done in Section IV. Finally, the Conclusions are presented in Section V.

II. The 3T pixel structure

The basic 3T pixel structure is depicted in Fig. 1. It contains, besides the photodiode, a Reset transistor (M_{RST}), a readout transistor (M_{SF}) and a row selection transistor (M_{SEL}). A biasing transistor, M_B, is placed in the bottom of each column of the pixel matrix, acting as a current source. M_{SEL} acts as an electronic switch: when ON (V_{SEL}=HIGH) it selects one specific pixel of the column. Neglecting the effect of 'ON' resistance of M_{SEL}, M_{SF} and M_B compose a typical source follower (SF) circuit, hence the naming of readout transistor as M_{SF}. Since the three transistors share the same substrate, the bodies of all of them are grounded, and omitted in the figure.

When a HIGH level Reset pulse is applied on the gate of M_{RST}, the junction capacitance of the reverse biased photodiode is charged, and v_{PIX} goes to $v_{RESET} - V_{tn(MRST)}$, where $V_{tn(MRST)}$ is the threshold voltage of M_{RST} and v_{RESET} is the voltage at the M_{RST} gate. The use of an NMOS device reduces the maximum possible v_{PIX} (e.g. the dynamic range), in exchange for greater fill factor, since a PMOS would require an N-well.

After Reset goes LOW, the collected photocurrent discharges the diode capacitance. At any given moment the output pixel voltage, v_{OUT}, is given by

$$v_{OUT} = v_{PIX} - V_{sat,SF} - V_{tn,SF} \tag{1}$$

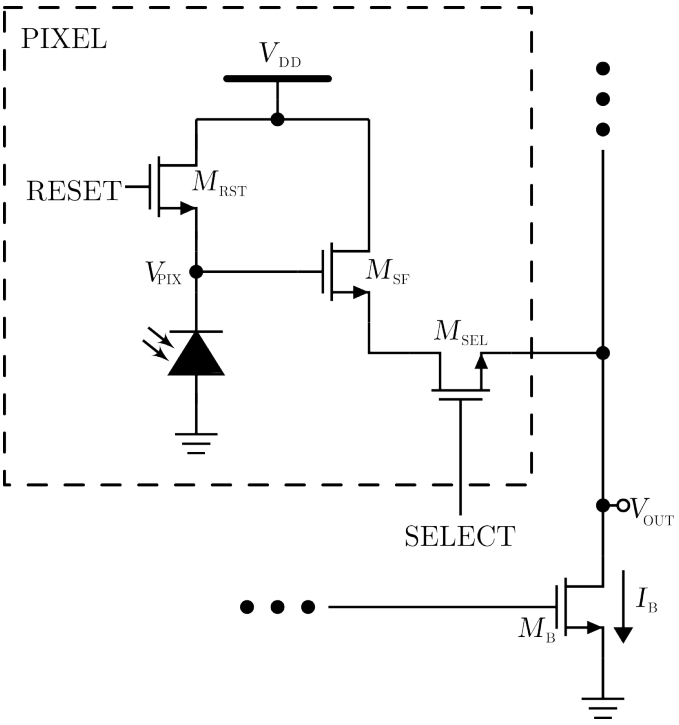

Fig. 1. 3T-APS structure.

Where $V_{sat,SF}$ and $V_{tn,SF}$ are, respectively, the saturation voltage and the threshold voltage of M_{SF}. Ideally $v_{PIX} - v_{OUT}$ (the SF offset voltage) should remain constant, but several factors (e.g. the body effect on $V_{tn,SF}$) lead the offset voltage to vary over the entire excursion of v_{OUT}, introducing a non-linear distortion. Thus, a nonlinear relation between v_{OUT} and v_{PIX} occurs.

The maximum output voltage swing, ΔV_{OUT}, is given by

$$\Delta V_{OUT} = (V_{DD} - V_{tn(RST)} - V_{tn,SF} - V_{sat,SF}) - V_{OV,B} \quad (2)$$

Where $V_{OV,B}$ is the overdrive voltage of the biasing transistor M_B.

Our aim is to improve the linearity of the achievable signal swing using different types of NMOS devices and voltage levels in a 3T pixel architecture.

A. Different configurations

The most common cases encountered in literature for the 3T-APS pixel use homogeneous transistors for the three transistors. However, if the process technology offers several NMOS devices, the combination of different kinds, associated with different supply, reset and/or select voltages can improve the output voltage swing.

Six possible combinations are investigated in this work. The Sky130 node offers several types of NMOS transistors (with their PMOS counterparts) [9]. Four NMOS devices are of interest for this study, as follows:

- 1.8V NMOS FET (1v8_std): the standard NMOS device for the Sky130 technology.
- 1.8V low-VT NMOS FET (1v8_lvt): NMOS devices with lower V_{tn}, due to V_{tn} adjust implants.
- 3.0V native NMOS FET (3v3_ntv): the native NMOS devices are constructed by blocking out all V_{tn} implants, leading to devices with very low threshold voltages. For Sky130 process, the minimum channel length for this device is $L = 0.5\ \mu m$.
- 5.0V/10.5V NMOS FET (5v0_std): devices capable of supporting $V_{GS(max)} = 5.5\ V$, $V_{BS(max)} = -5.5\ V$ and $V_{DS(max)} = 11\ V$. Minimum $L = 0.5\ \mu m$.

TABLE I
TRANSISTOR MODELS OF EACH CONFIGURATION

config.	M_{RST}	M_{SF}	M_{SEL}
I	1v8_std (1/0.2)[a]	1v8_std (1/0.4)	1v8_std (1/0.2)
II	1v8_lvt (1/0.2)	1v8_lvt (1/0.4)	1v8_lvt (1/0.2)
III	1v8_lvt (1/0.2)	3v3_ntv (1/0.5)	5v0_std (1/0.5)
IV	5v0_std (1/0.5)	5v0_std (1/0.5)	5v0_std (1/0.5)
V	5v0_std (1/0.5)	3v3_ntv (1/0.5)	5v0_std (1/0.5)
VI	5v0_std (1/0.5)	3v3_ntv (1/0.5)	5v0_std (1/0.5)

[a]Aspect ratio (W/L) in ($\mu m/\mu m$).

TABLE II
HIGH VOLTAGE LEVELS OF EACH CONFIGURATION

config.	$V_{DD}\ (V)$	$V_{RESET}\ (V)$	$V_{SEL}\ (V)$	$V_{PIX}\ (V)$
I	1.8	1.8	1.8	1.5
II	1.8	1.8	1.8	1.7
III	1.8	1.8	3.3	1.7
IV	3.3	3.3	3.3	2.6
V	3.3	3.3	3.3	2.6
VI	3.3	3.3	5.0	2.6

For an NMOS device operating as a switch with $V_{GS} = 3.3\ V$, the 5v0_std must be used, as the process does not provide a specific 3.3 V device different from the native transistor.

The six configurations are described in Table I, where the device type and its respective aspect ratios are shown for M_{RST}, M_{SF} and M_{SEL}. Table II shows the values for supply voltage, V_{DD}, the high level voltage for V_{RESET} and V_{SEL}, as well as the maximum value of V_{PIX}, in this case, obtained by simulation of the operating point, using models supported by the PDK. The photodiode was replaced by a linear capacitor.

For all the cases, a biasing current $I_B = 2\ \mu A$ was used, set by the biasing transistor, M_B, a 5v0_std NMOS, with $W = L = 1.0\ \mu m$. Its overdrive voltage for the rated current, given by simulation, is close to $152\ mV$.

The use of native devices for the readout transistor in Configurations III, V and VI aims to minimize the offset from V_{PIX} to V_{OUT}. Such use of a native device can be found in a 4T configuration in [10], in this case, investigating the noise reduction that can be achieved with the native transistor. In another example, both Reset and readout transistors are native NMOS devices, for a 3T pixel [11]. This would raise V_{PIX} after Reset, extending the signal excursion, at a first glance. However, the use of a native device for M_{RST} was not considered in this work. Since the native NMOS does not

completely turn off, it would charge continuously the photodiode capacitance with a small current, even with $V_{RESET} = 0$, leading to higher values of dark current and impairing the pixel readout for low illumination levels.

III. Simulation Results

The circuit configurations were simulated in NGSPICE, by using the Sky130 PDK device models available in [9]. In order to evaluate the nonlinearity and voltage swing, a DC sweep analysis was applied, replacing M_{RST} by an ideal voltage source, ranging from zero to V_{PIX}.

Various approaches for evaluating nonlinearity are reported in the literature, such as the least squares error or the coefficient of determination [12]. The total harmonic distortion (THD) was used as a parameter to measure nonlinearity in a CMOS image sensor paper [13]. However, for this study, a metric that evaluates how similar are variations in V_{OUT} w.r.t. V_{PIX} is proposed, considering variations in the gate-source voltage of M_{SF}, $V_{GS,SF}$, hereafter referred to simply by ΔV_{GS}, and considering the total output voltage swing, ΔV_{OUT}. A figure of merit can be proposed, measuring, for each simulation, the ratio $\Delta V_{GS}/\Delta V_{OUT}$, thus indicating that the lower ratio is an effective measure of the linearity of the pixel compared to its output range.

The DC Sweep results for the six configurations are depicted in Fig. 2. For didactic purposes, the horizontal axes were inverted, starting from the value of V_{PIX} after Reset, shown in Table II. This mimics the transient response after $V_{RESET} = 0$, when the photocurrent is integrated, and can give a valuable insight for a comparative analysis.

Table III shows the values of the coefficient of determination between V_{OUT} and V_{PIX}. The values of $V_{OUT(max)}$, ΔV_{OUT}, ΔV_{GS} (in V) and $\Delta V_{GS}/\Delta V_{OUT}$ (in V/V) were tabulated in Table IV.

TABLE III
Coefficient of Determination

config.	$R^2(\%)$
I	99.9914
II	99.9954
III	99.9979
IV	99.9865
V	99.2671
VI	99.9981

TABLE IV
Simulation Results

config.	$V_{OUT(max)}$	ΔV_{OUT}	ΔV_{GS}	$\Delta V_{GS}/\Delta V_{OUT}$
I	0.674	0.522	0.117	0.224
II	0.961	0.809	0.130	0.161
III	1.473	1.321	0.256	0.194
IV	1.457	1.305	0.290	0.222
V	2.027	1.875	0.317	0.169
VI	2.347	2.195	0.318	0.145

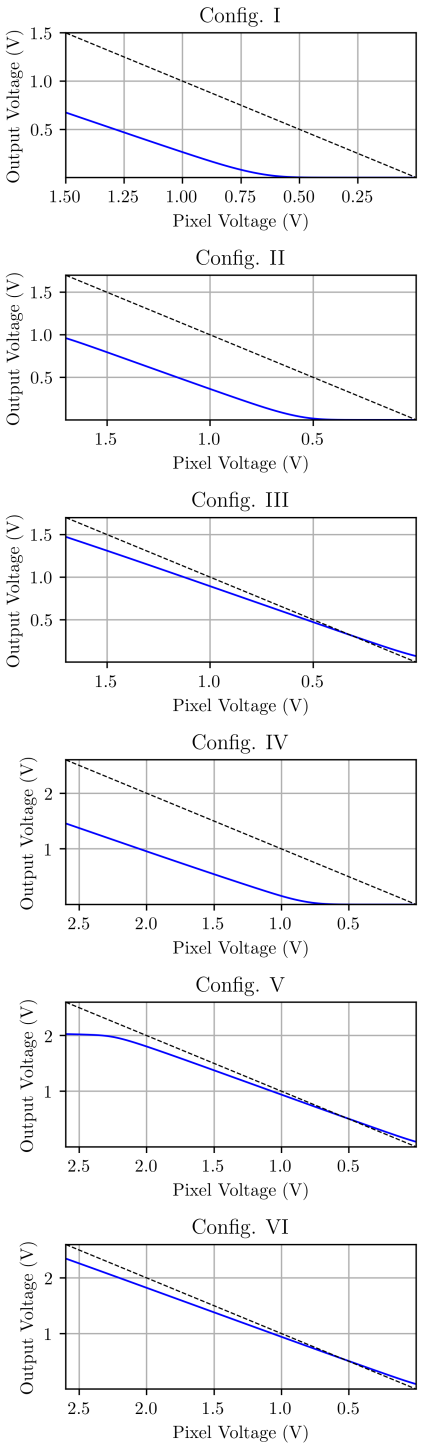

Fig. 2. DC Sweep results. Gray: pixel voltage; Blue: output voltage.

IV. Discussion

As shown in Table IV, the configurations that use the native transistor for readout (configurations III, V, and VI) exhibit the largest voltage swing at the output for a given maximum V_{PIX} value. However, this comes at the cost of increased gate-source voltage variations in the M_{SF}, which compromise the output

linearity.

Configuration V demonstrates the worst linearity because the selection transistor M_{SEL} changes the operation from triode region to the saturation region at high V_{OUT} values. This makes this approach impracticable due to significant sensitivity loss in low-light environments and also precludes the adoption of correlated double sampling (CDS), which is used to reduce fixed-pattern noise (FPN). However, by using a high level voltage V_{SEL} of $5.0\ V$, we prevent the selection transistor M_{SEL} from operating in the saturation region and achieve configuration VI, which has the largest voltage swing and the highest coefficient of determination.

In fact, Configurations III and VI share a similar principle: the use of native transistor for M_{SEL} and the gating M_{SEL} with a voltage higher than V_{DD} (and consequently V_{PIX}), in order to maintain the selection transistor in the linear region when turned on. If one compares the coefficient of determination, the output swing and the parameter $\Delta V_{GS}/\Delta V_{OUT}$, configuration VI could be the more advantageous of the six presented. However, from a practical point of view, it must be realized that a 5 V signal would be required only for improving the pixel linearity, since it will not be used in other circuit of the signal path. This could represent a technically less attractive solution.

Moreover, it is interesting to note that an output voltage higher than the pixel voltage is exhibited for low values of V_{PIX} when using the native transistor. This confirms that a native device does not fully turn off, and contributes to the non-linearity in Configurations III and VI, even considering that the proposed metrics seem favorable for these configurations.

V. Conclusion

In this paper, the linearity and output voltage swing of the 3T pixel using different MOSFET models available in the open-access Sky130 PDK and applying different supply, reset, and row select voltages were investigated.

To compare the results obtained with NGSPICE, we proposed measuring the variation in the gate source voltage of M_{SF} relative to the output swing, along with the coefficient of determination.

The results showed that using the native transistor available in Sky130 allowed for a significant increase in the pixel output range. However, to maintain linearity in the pixel response, it was necessary to apply a gate voltage to the selection transistor that was greater than the normal supply voltage. This approach may not be a technically attractive solution when a 5.0 V voltage source is required solely to improve linearity.

As the dynamic range of the pixel is determined both by the maximum signal excursion and by the noise floor, the study of noise levels in the different configurations presented will be the focus of our future work, continuing the development of a complete pixel array using the open-source tools available for working with the Sky130 PDK.

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